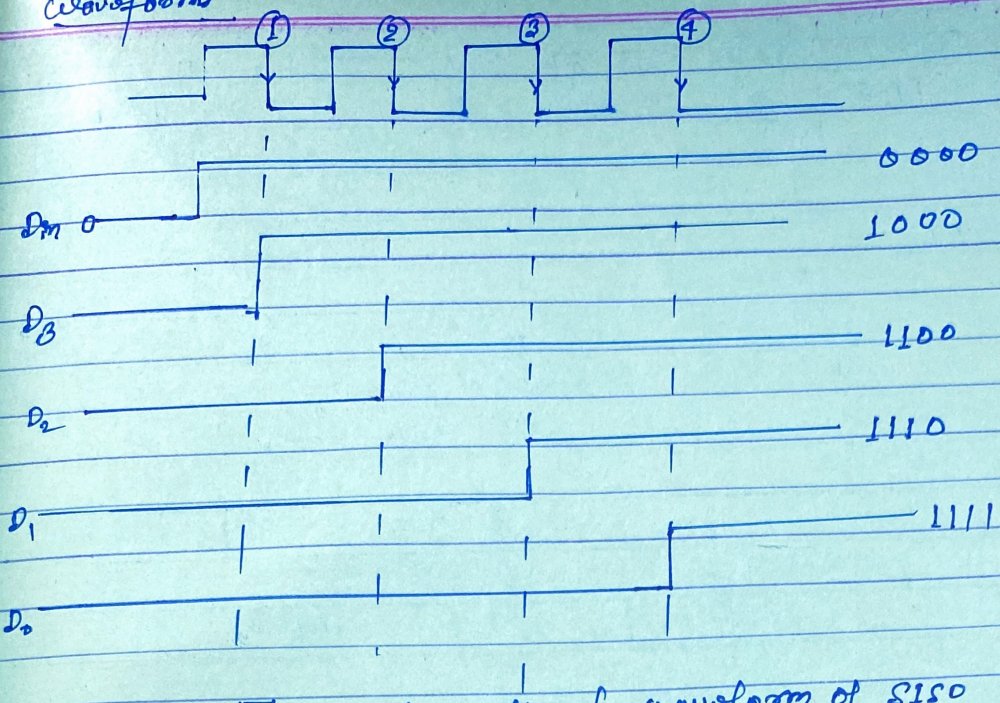

Fig: Operational waveform of SISO.

Serial Input parallel Output

Serial Input parallel Output (SIPO)

The register in which the data is loaded serially one by one and output is taken out at a time (simultaneously), the register is called SIPO. register.

In SIPO register, the outputs are register disabled as load or the loading is taking place. As soon as the loading is complete, the output are enabled so that all the loaded data is made available over all the output lines simultaneously.

The no. of clock required to store the n-bit data is n clock cycle. This means the speed of SIPO is same as the same or that of SIP SISO.

The functional block diagram of SIPO is shown on the overleaf page.

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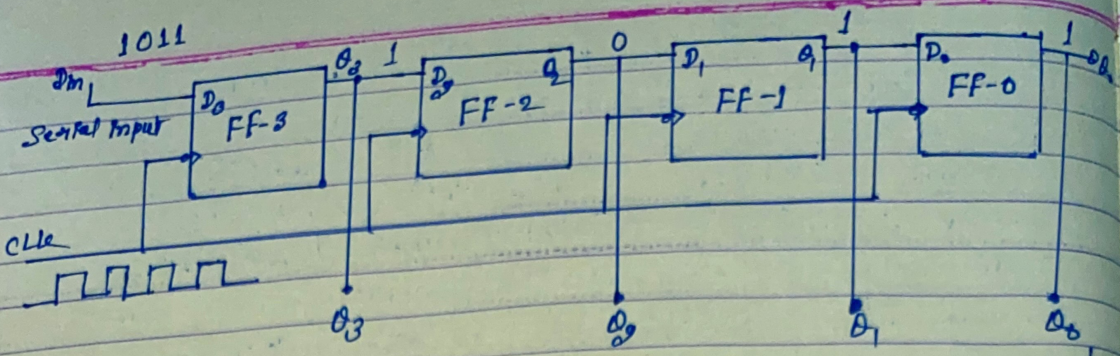

Fig: SIPO shift register

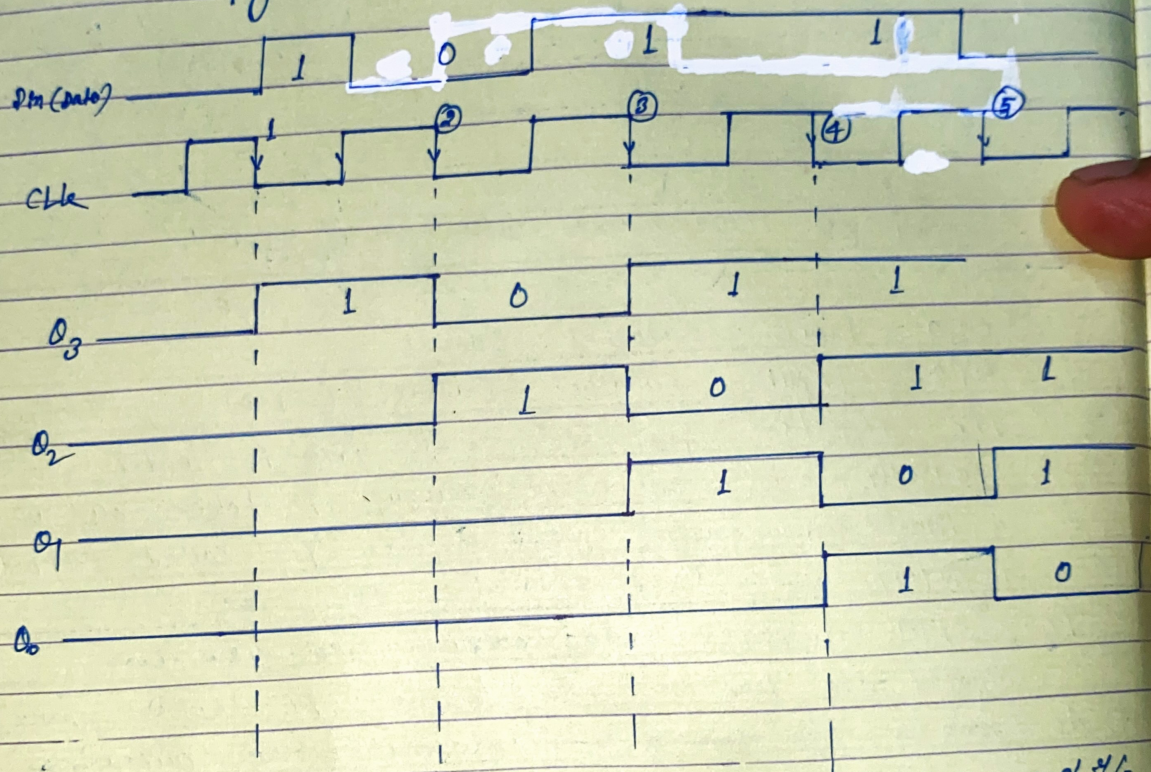

Fig: waveform of register.

Truth Table:

clk	Dm	output Q_3	Q_2	Q_1	Q_0
↓	0	0	0	0	0
↓	1	1	0	0	0
↓	1	1	1	0	0
↓	0	0	1	1	0
↓	1	1	0	1	1
↓					
↓					

③ PARALLEL IN SERIAL OUTPUT (PISO):-

In this circuit mode, the bits are entered in parallel fashion and output is taken serially bit by bit. Output of previous FF is connected to the input of the next one with the help of a combinational circuit. Then, the binary input word $B_0, B_1, B_2 B_3$ is applied through the same combinational circuit. There are two modes in which the circuit works. There are i) Shift mode ii) Load mode.
The below figure shows the block diagram of PISO.

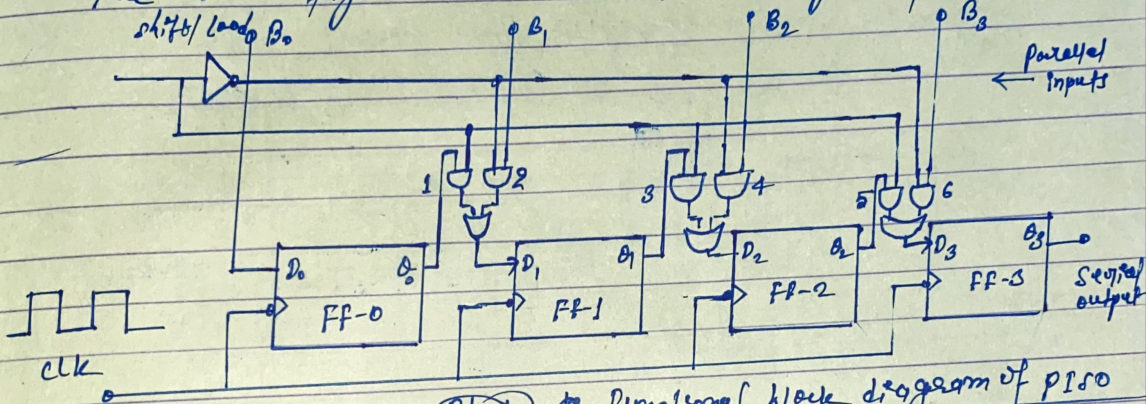

Fig: (Block) & functional block diagram of PISO

Operation:

Load Mode:- when the shift/load line is low (0), the AND gate 2, 4, 6 become active. They pass B_1, B_2 and B_3 bits to the corresponding flip-flop. On low going edge of clock, the binary inputs B_0, B_1, B_2 and B_3 gets loaded into the corresponding flip-flop. Therefore parallel loading take place.

Shift Mode: when the shift/load line is high (1). the AND gates 2, 4, 6 becomes inactive and hence parallel loading of data is impossible. But the AND gates 1, 3, 5 becomes active. Therefore the shifting of data from left to right bit by bit on application of ~~one~~ -ve falling edge of clock signal takes place.

(4) PARALLEL IN PARALLEL OUT (PIPO).

In this type of shift register the data is ~~serially~~ parallelly loaded simultaneously and output is also parallelly taken. In this mode, the 4-bit binary input B_0, B_1, B_2, B_3 is applied to the data inputs D_0, D_1, D_2, D_3 respectively of the four flip-flops. As soon as a negative clock edge is applied, the input binary bits will be loaded into the flip-flops simultaneously. The loaded bits will appear simultaneously to the output side.

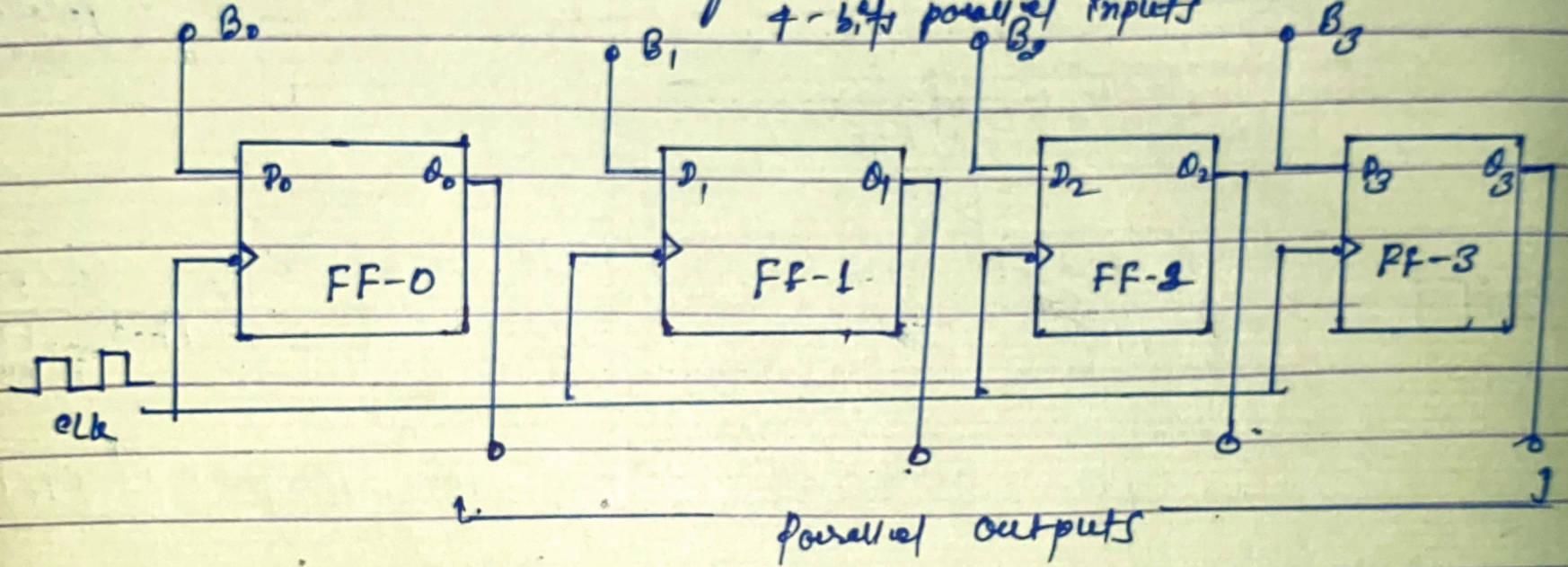

Fig: parallel inputs parallel outputs (PIPO).